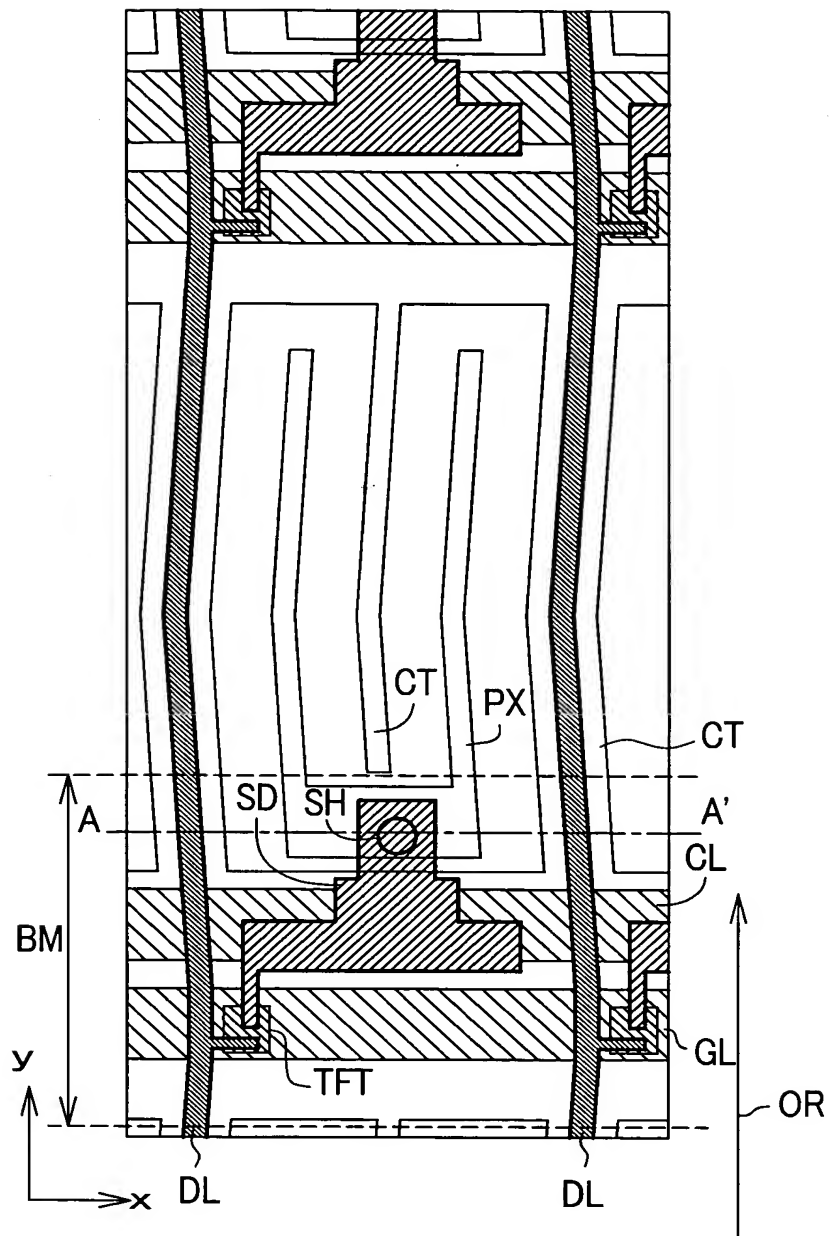


*FIG. 1A*



*FIG. 1B*

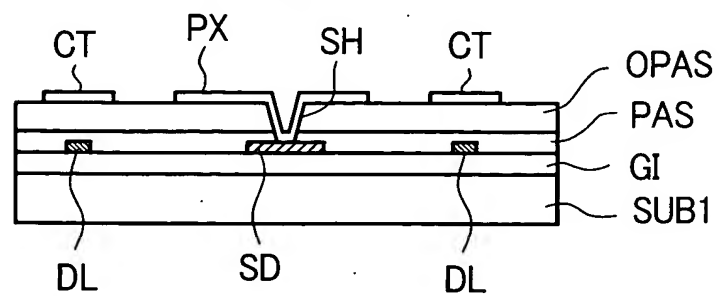
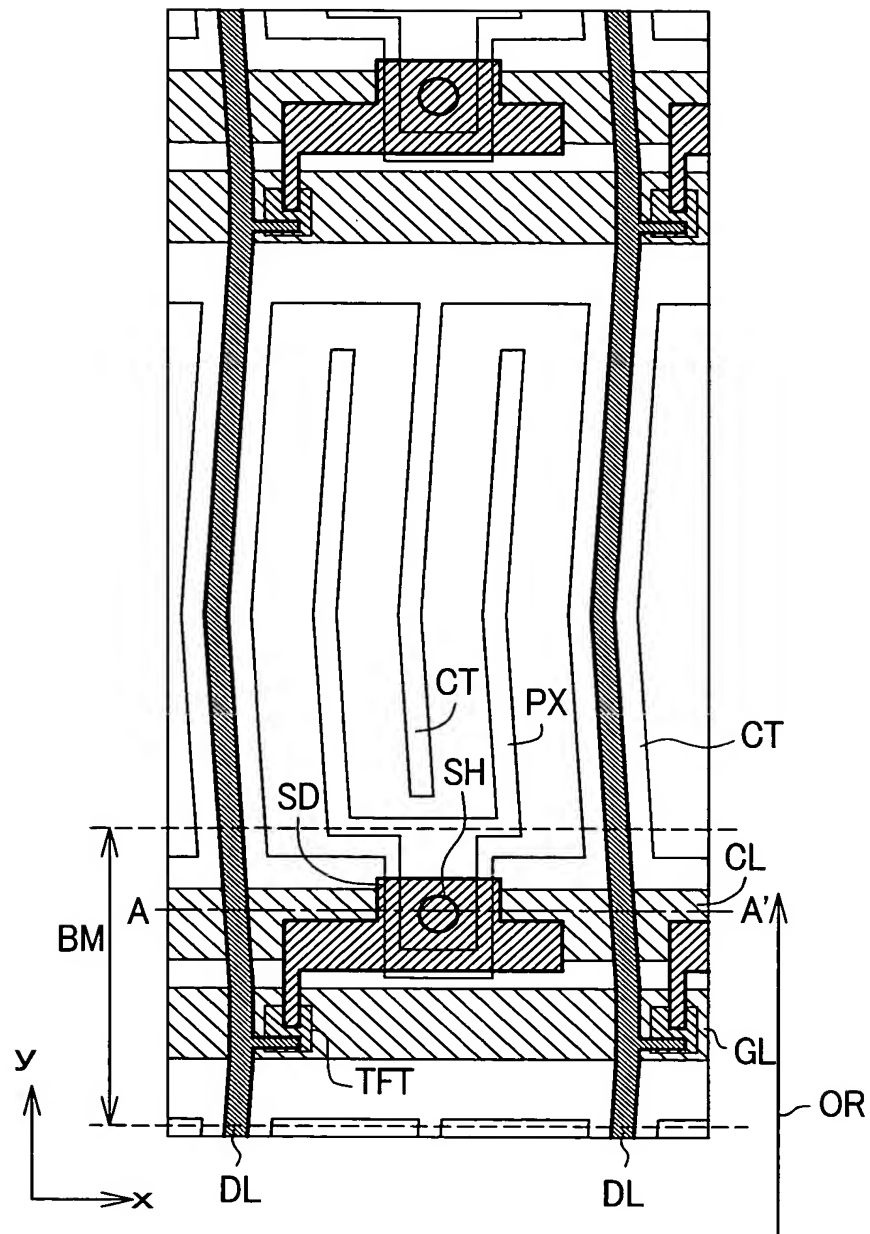


Fig. 1 is a cross-sectional view of a semiconductor device. The device is built on a substrate. A gate layer (GL) is formed on the substrate. A TFT layer is formed on the GL. A central region is defined by a gate (SD) and a gate (SD2). A central region is defined by a gate (SD) and a gate (SD2). A central region is defined by a gate (SD) and a gate (SD2).

A cross-sectional view of a semiconductor device. The structure consists of several layers: a top layer labeled 'E', a layer labeled 'CT' (with a curved arrow pointing to it), a layer labeled 'PX', and a stack of three layers labeled 'OPAS', 'PAS', and 'GI' from top to bottom. The bottom-most layer is labeled 'SUB1'. A contact region labeled 'CL' is shown on the left side, extending through the 'E', 'CT', and 'GI' layers to the 'SUB1' layer.

A cross-sectional view of a semiconductor device. The structure consists of a substrate layer labeled SUB1. Above SUB1 is a gate insulating layer labeled GI. On top of GI is a passivation layer labeled PAS. The topmost layer is an organic passivation layer labeled OPAS. A contact layer labeled CT is located on the OPAS layer. An electrode labeled E is formed on the CT layer. A source-drain region labeled SD1 is formed in the CT layer, and a channel layer labeled CL is formed in the GI layer. The SD1 and CL regions are shown with hatching.

*FIG. 3A*



*FIG. 3B*

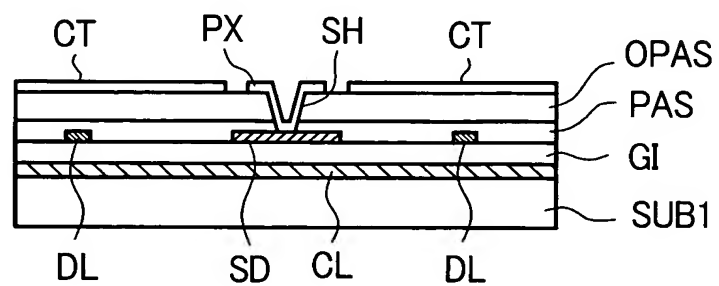
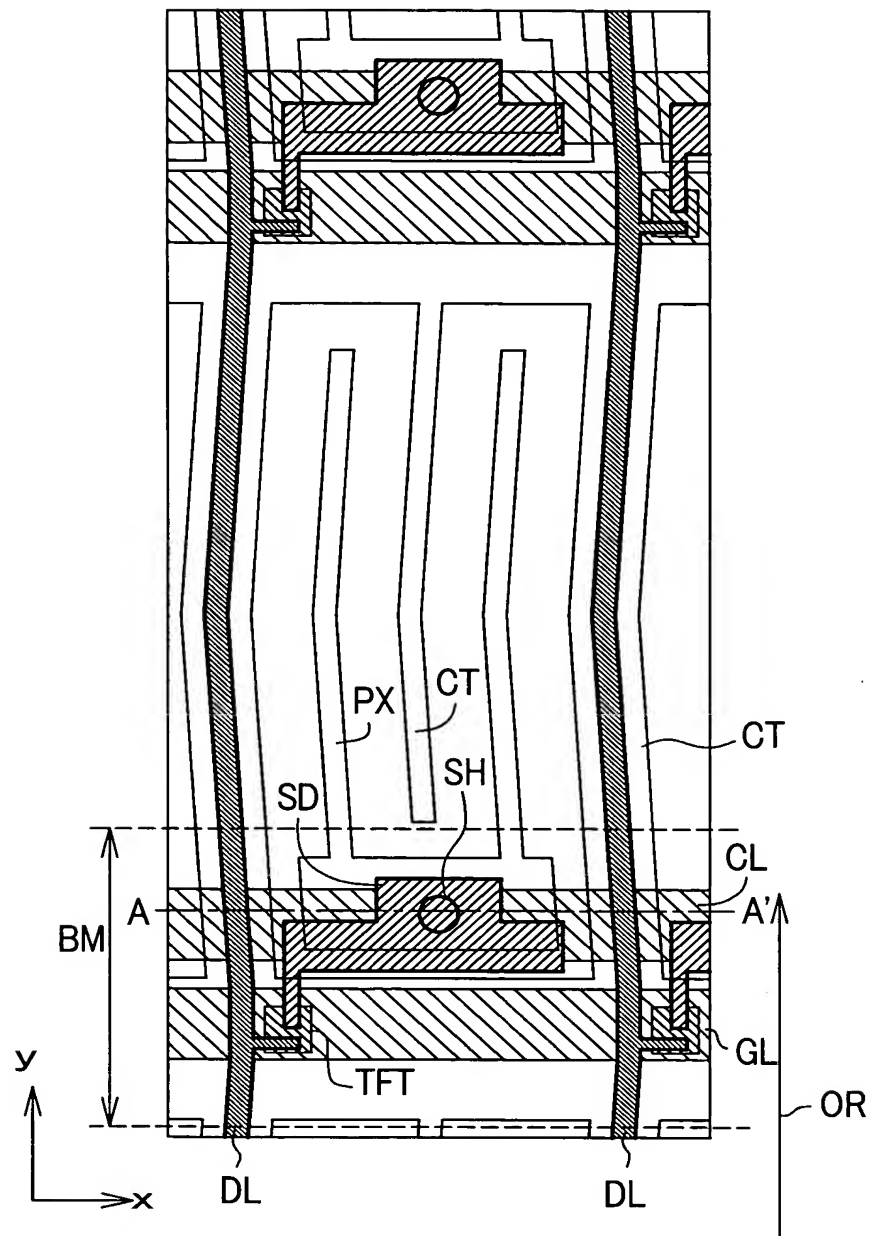
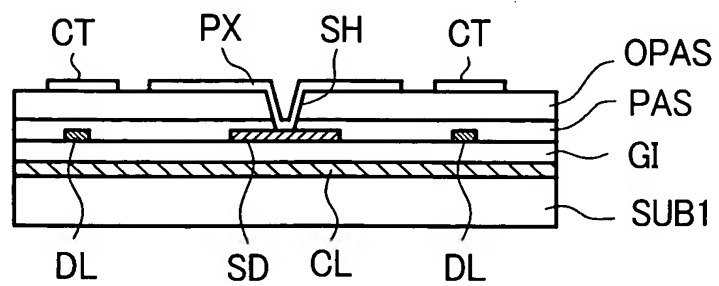


Fig. 1 is a cross-sectional view of a pixel structure. It shows a TFT (Thin Film Transistor) structure on a substrate. The TFT includes a gate line (GL) and a data line (DL). The structure is covered by a passivation layer (PX) and a protective layer (CT). A central region (B) contains a circular element (C). Other layers include SH (Semiconductor), SD (Source/Drain), and SD3 (Source/Drain). Dimensions a, b, and c are indicated for specific features.

*FIG. 5A*



*FIG. 5B*



*FIG. 6*

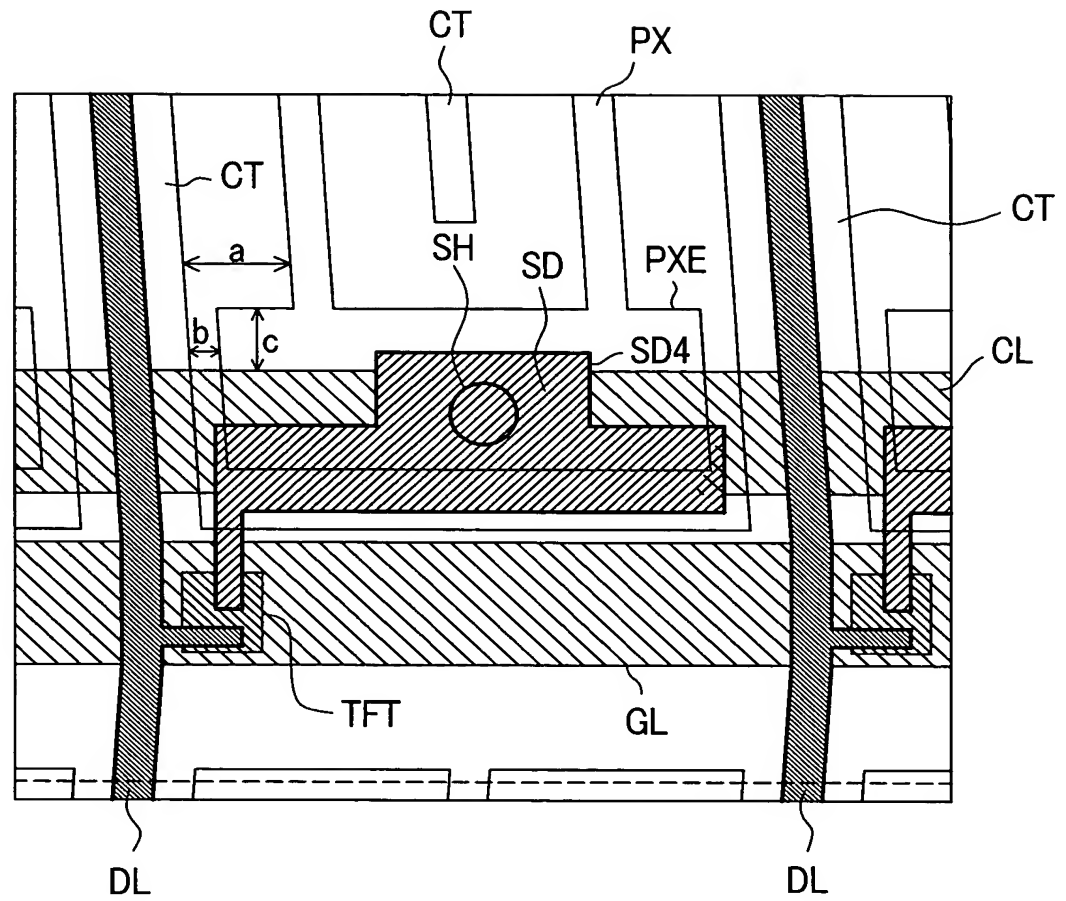
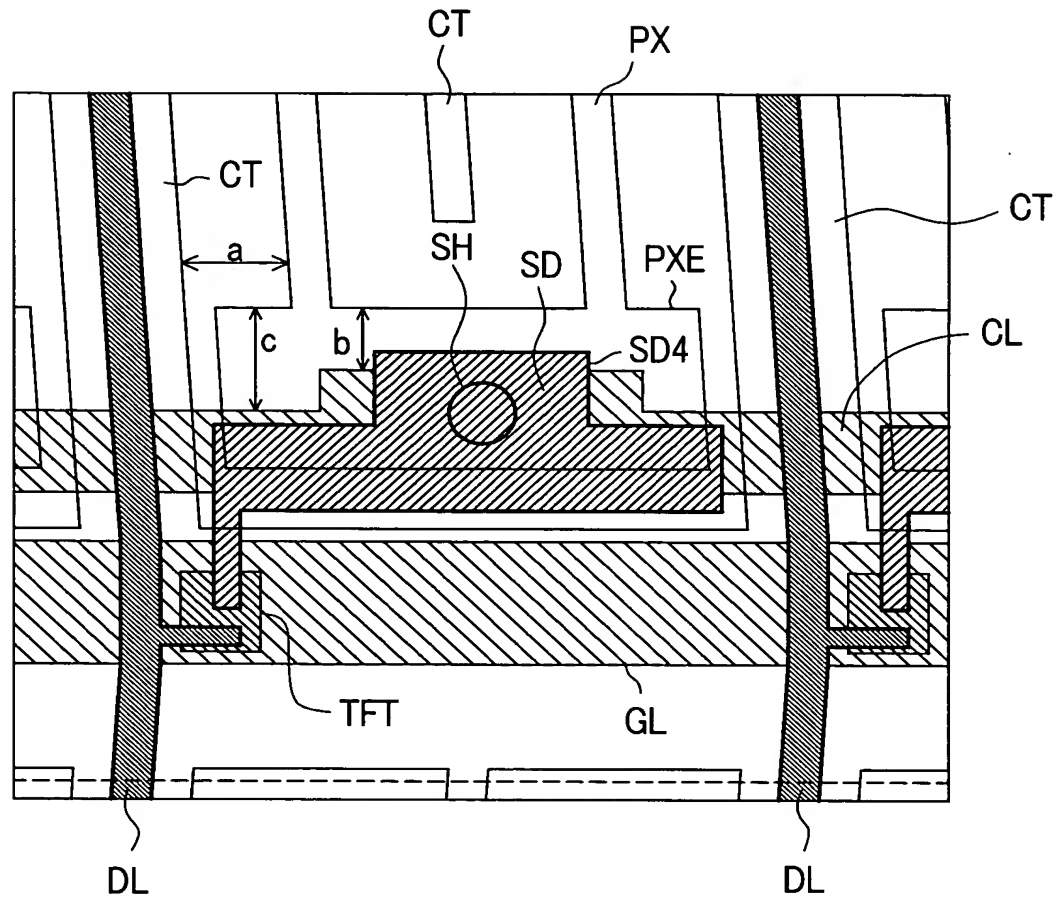


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate (SUB1) with a stack of layers: DL (dielectric layer), SD (semiconductor layer), CL (conductive layer), and GI (gate insulator). A passivation layer (PAS) is formed over the substrate. The PAS has openings for contacts (CT) and a probe (PX). A shield (SH) is positioned over the probe opening. An organic passivation layer (OPAS) is formed on the top surface of the device.

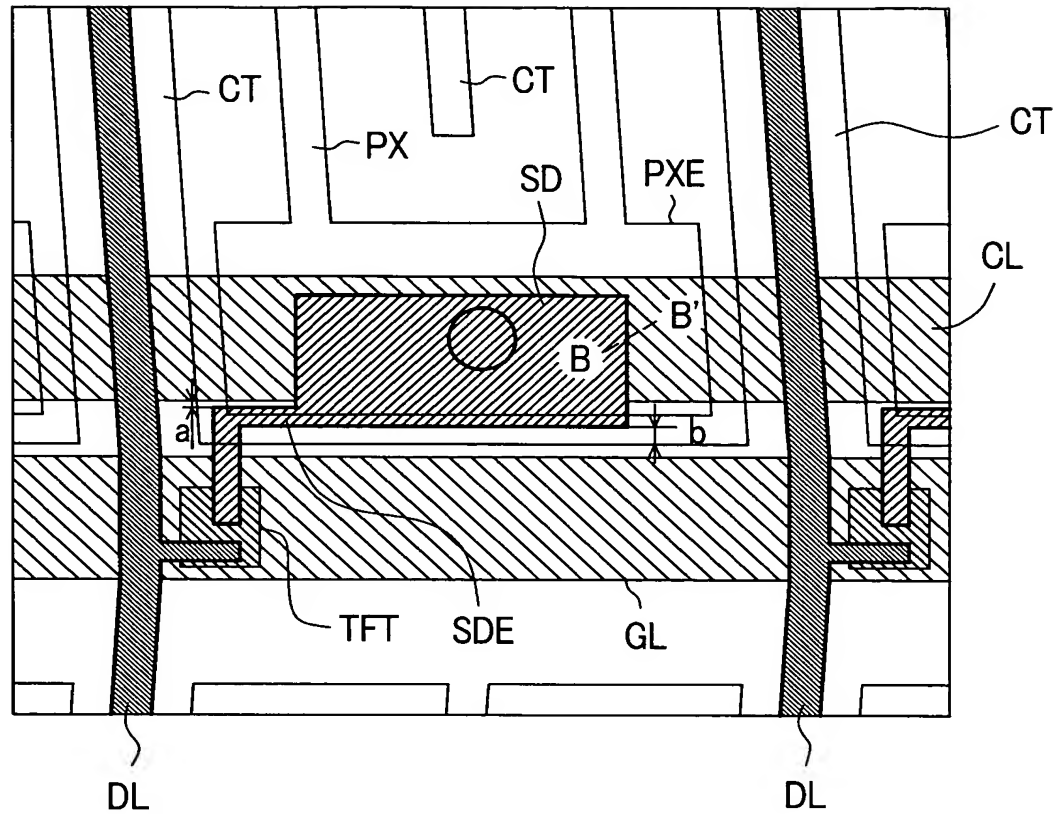
*FIG. 8*



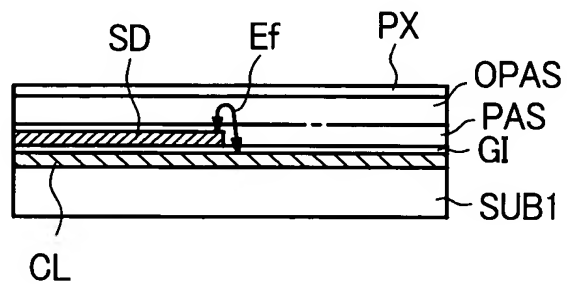


A detailed cross-sectional diagram of a liquid crystal display assembly. The diagram shows a central liquid crystal layer (CL) sandwiched between two glass substrates (GL). The top substrate features a pixel electrode (PX) and a common electrode (CT). The bottom substrate features a pixel electrode (PX), a common electrode (CT), and a thin-film transistor (TFT). A spacer (SD) is used to maintain the gap between the substrates. The assembly is sealed with a sealant (DL) and a frame (BM). A coordinate system (x, y) is shown at the bottom left, and a vertical arrow (A) indicates the viewing direction. The label 'OR' is at the bottom right.

Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate (SUB1) with a gate insulating layer (GI) and a passivation layer (PAS) on top. A central trench is filled with a semiconductor layer (SH). The trench is flanked by a polysilicon layer (PX). The outer edges are covered by a contact layer (CT). The device also includes a diffusion layer (DL), a source/drain region (SD), and a channel region (CL).



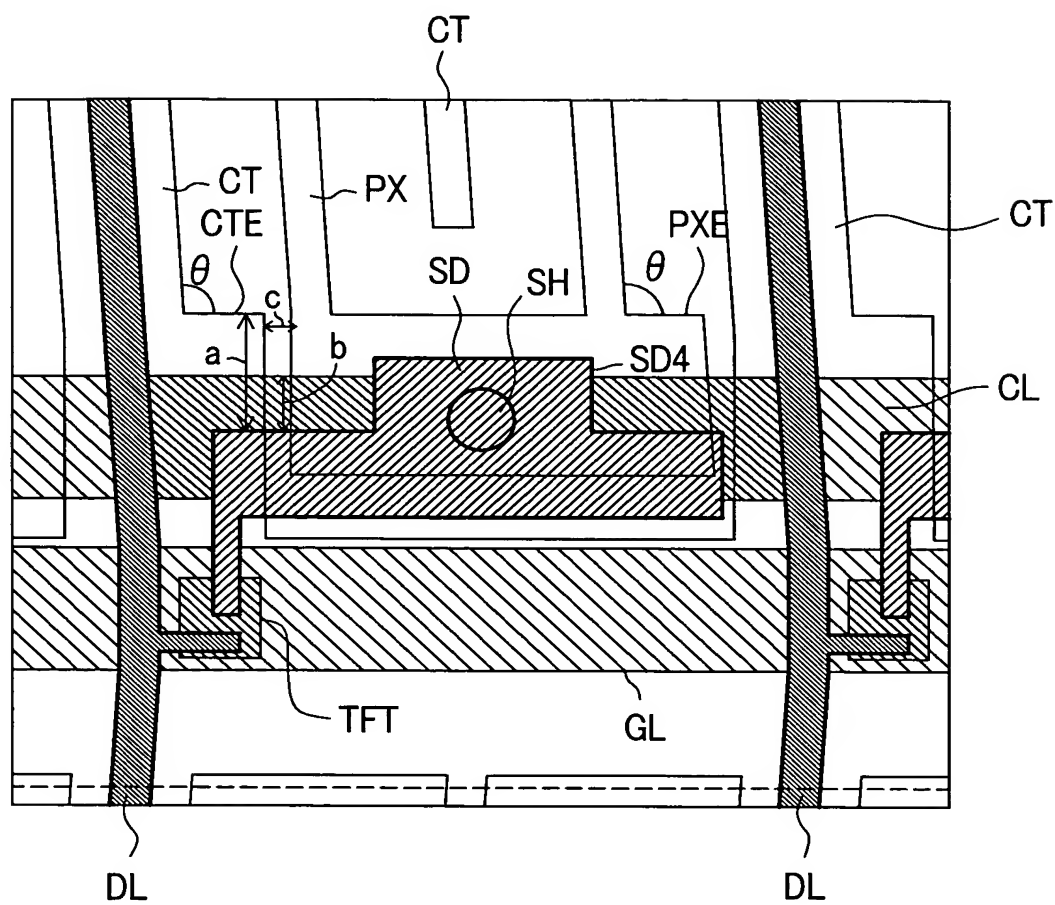
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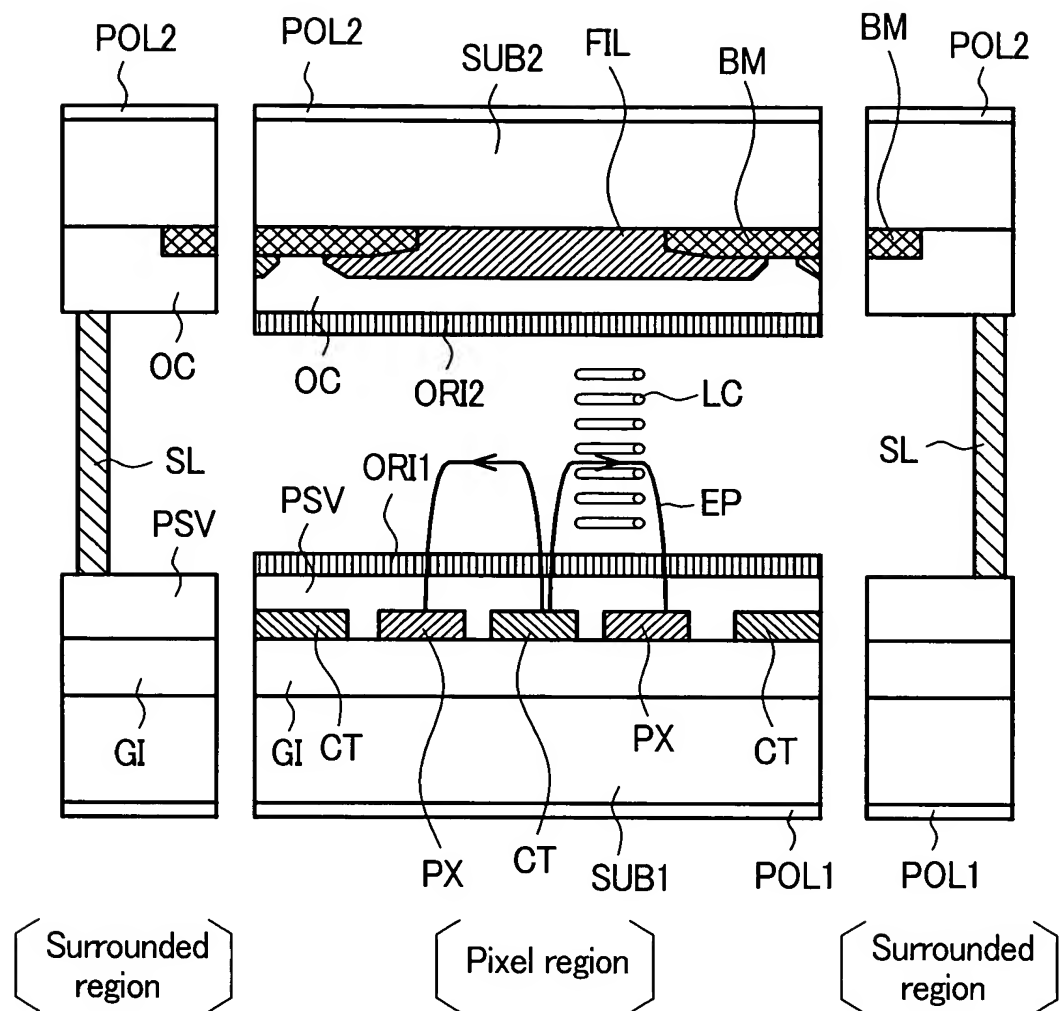
[illegible]

Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate (SUB1) with a series of layers (DL, SD, CL, DL) and a gate stack (GI, PAS, OPAS). The gate stack is patterned into regions labeled CT, PX, SH, and CT. The central region (SH) is a shallow trench.

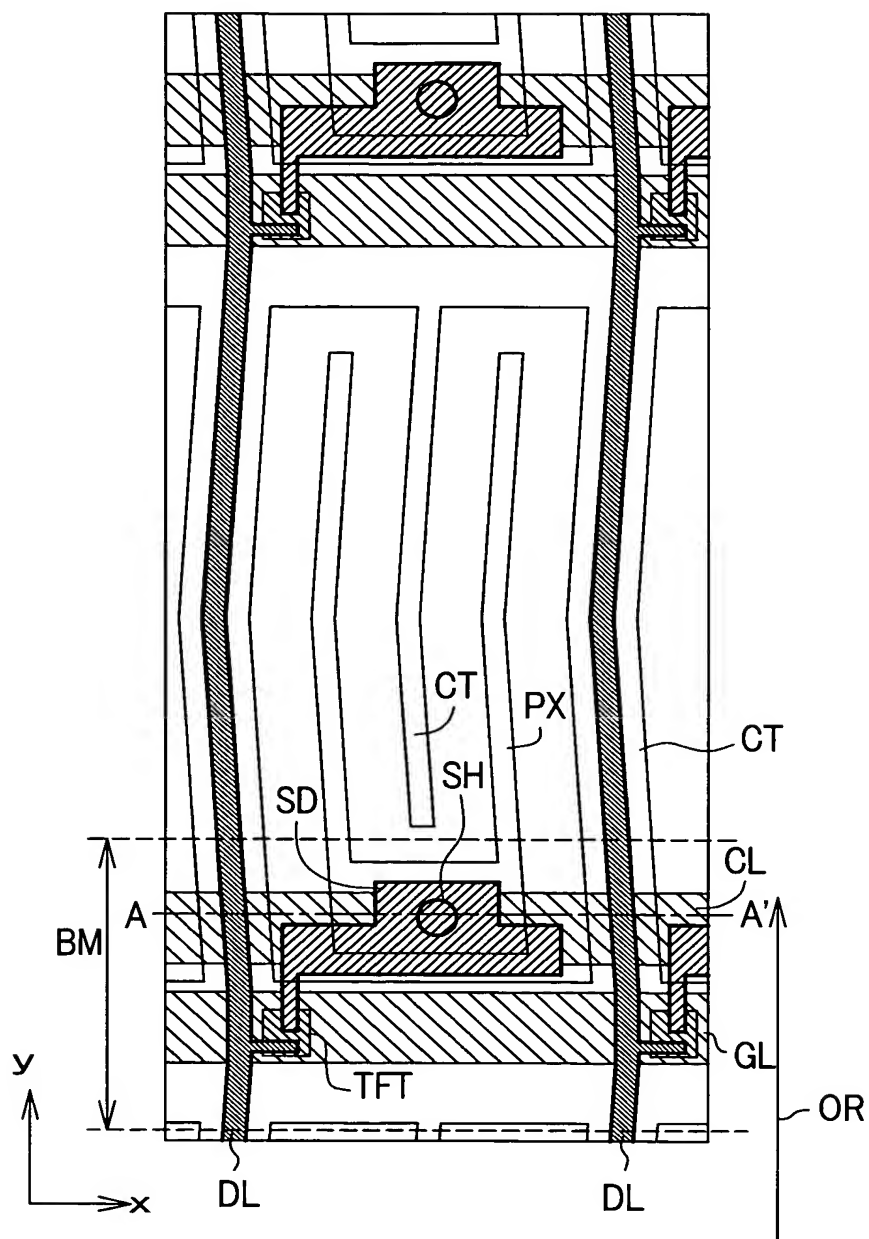
*FIG. 12*



*FIG. 13*



*FIG. 14A*



*FIG. 14B*

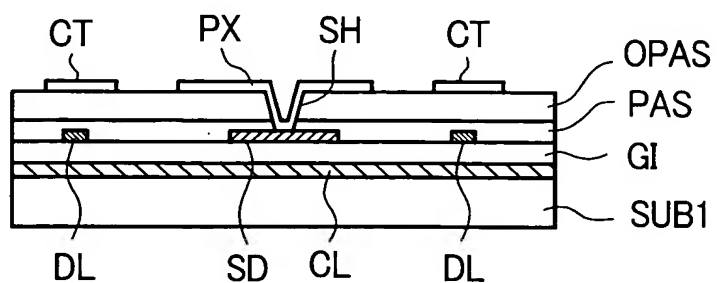


Diagram illustrating a cross-sectional view of a semiconductor device. The structure includes a substrate (SUB1) with layers GI, PAS, and OPAS. A conductive layer CL is shown on the left, and a pixel (PX) is shown on the right. An electric field E is indicated by a curved arrow between CL and PX.